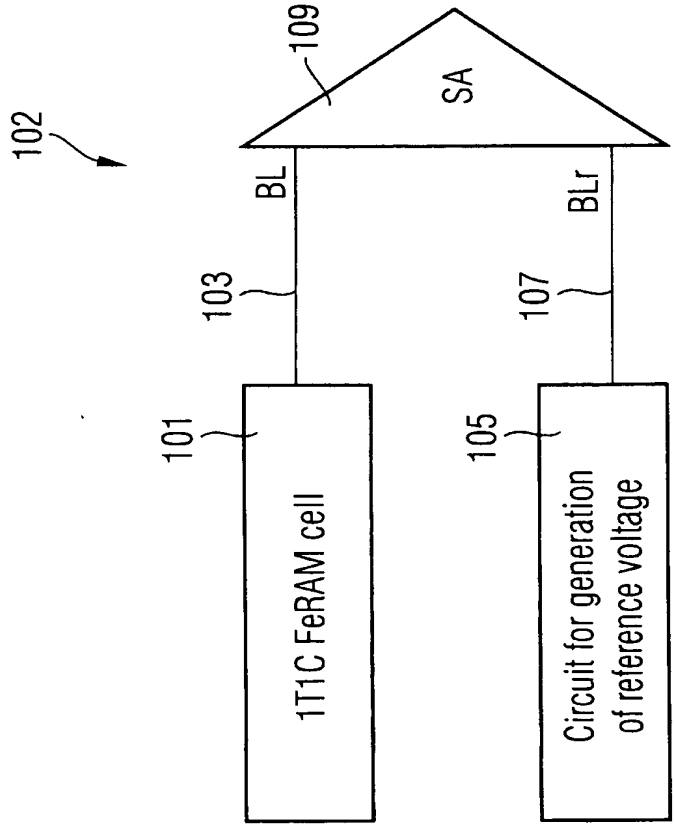

FIG 1
Prior Art

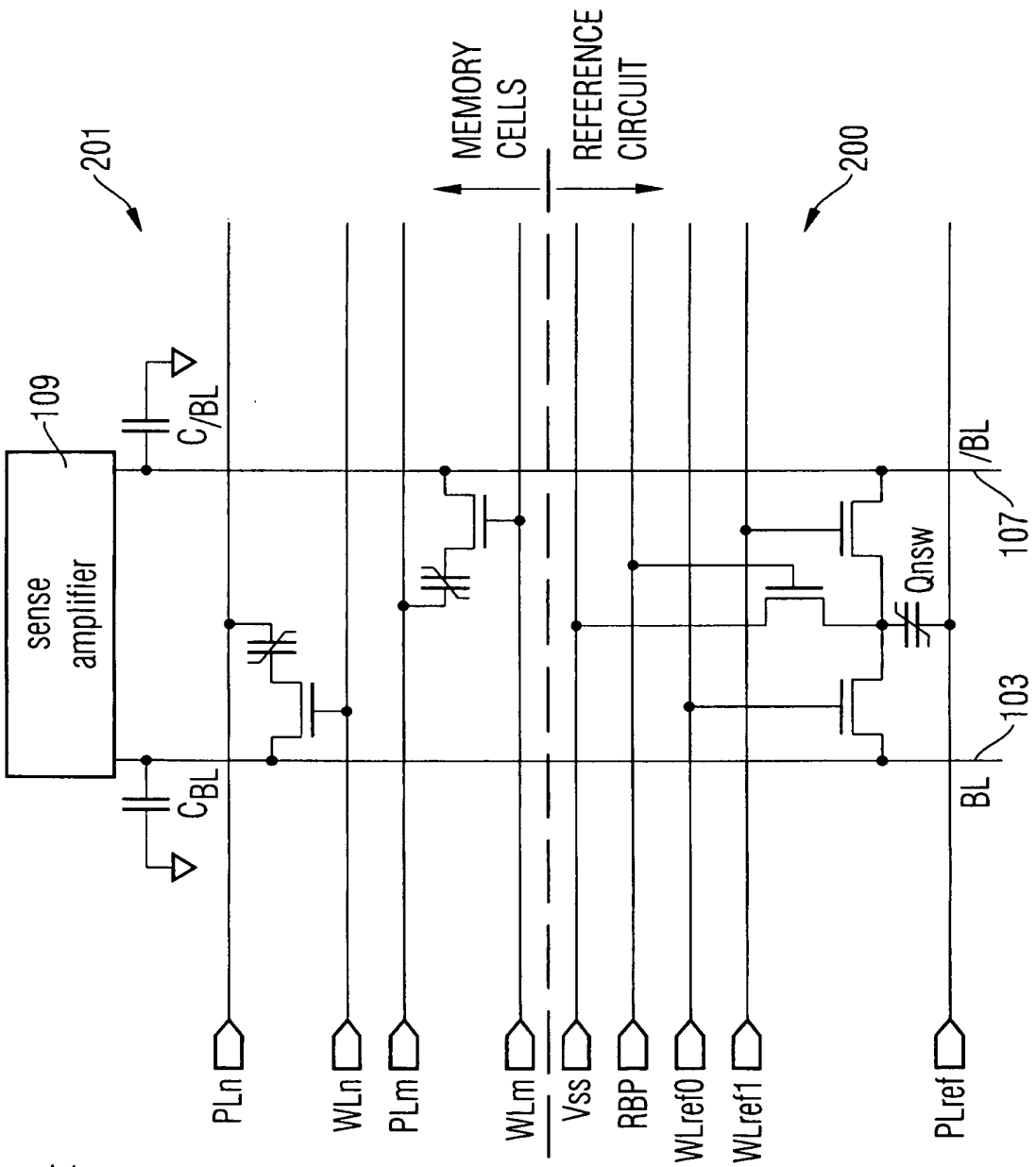

FIG 2
Prior Art

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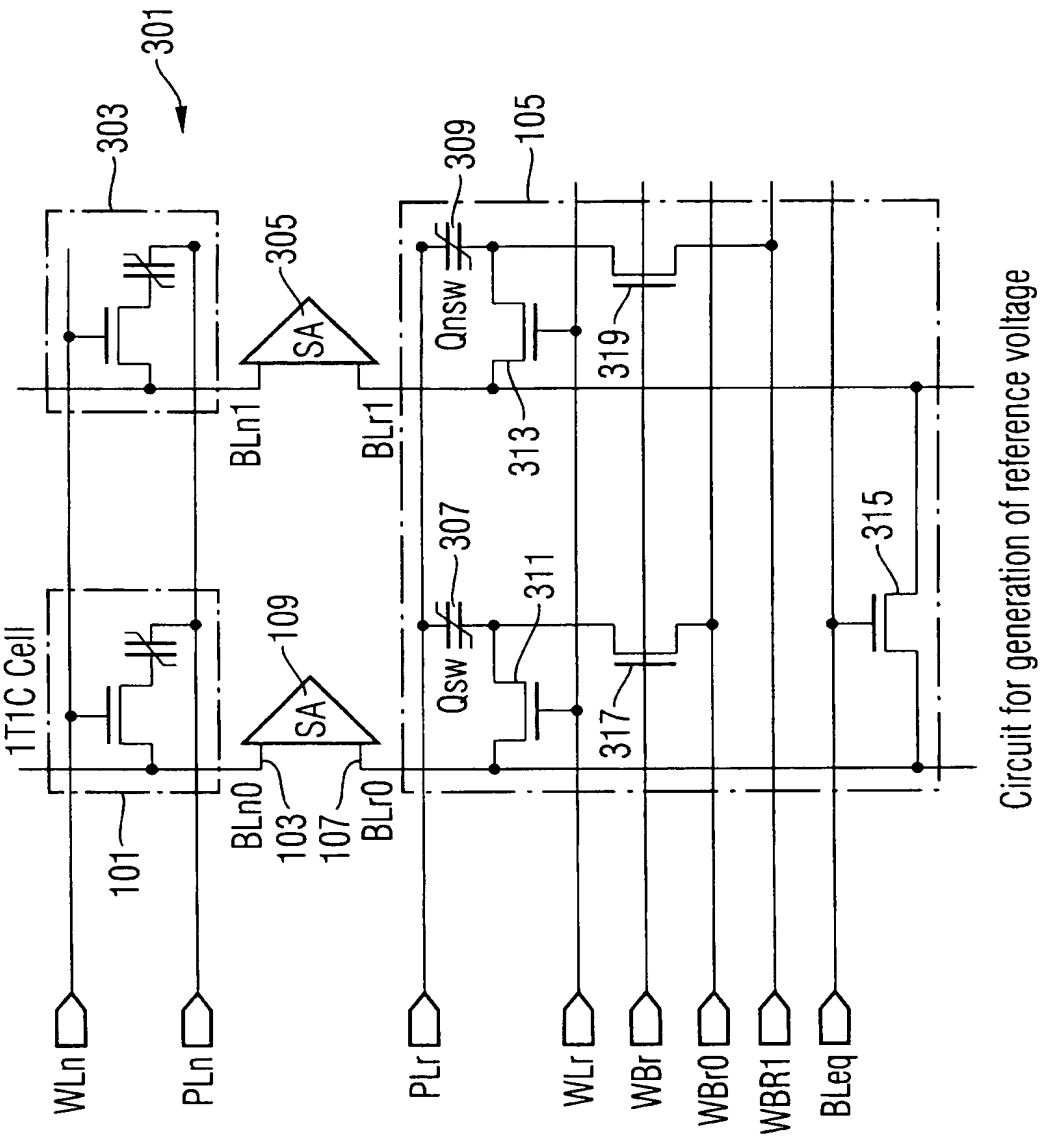
301
303
305
309
105
SA
Qnsw
319
313
BLn1
BLr1
1T1C Cell
109
307
311
315
SA
Qsw
317
101
BLn0
103
107
BLr0
WLn
PLn
PLr
WLr
WBr
WBr0
WBR1
BLeq
Circuit for generation of reference voltage

FIG 3

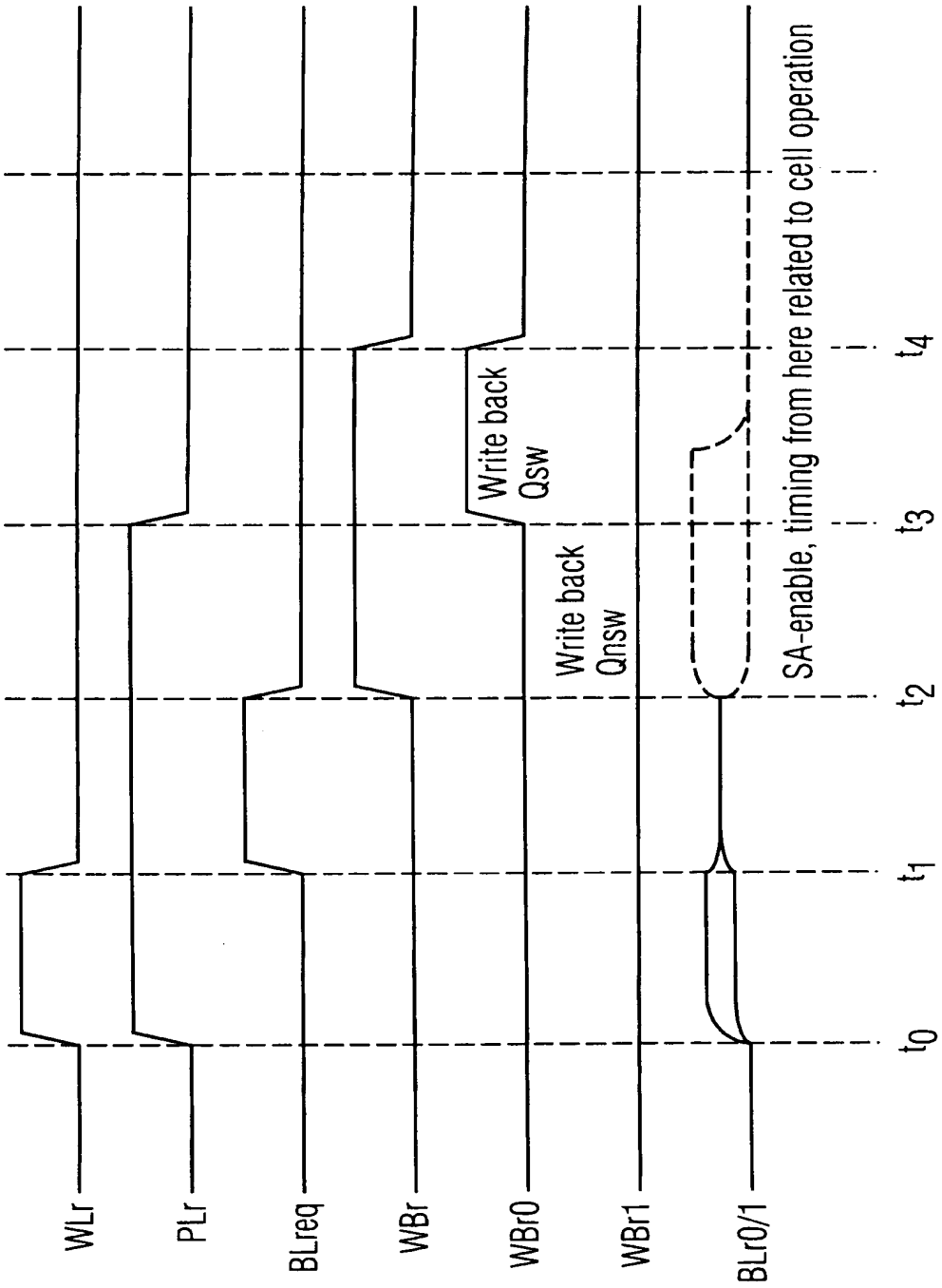

FIG 4
Prior Art

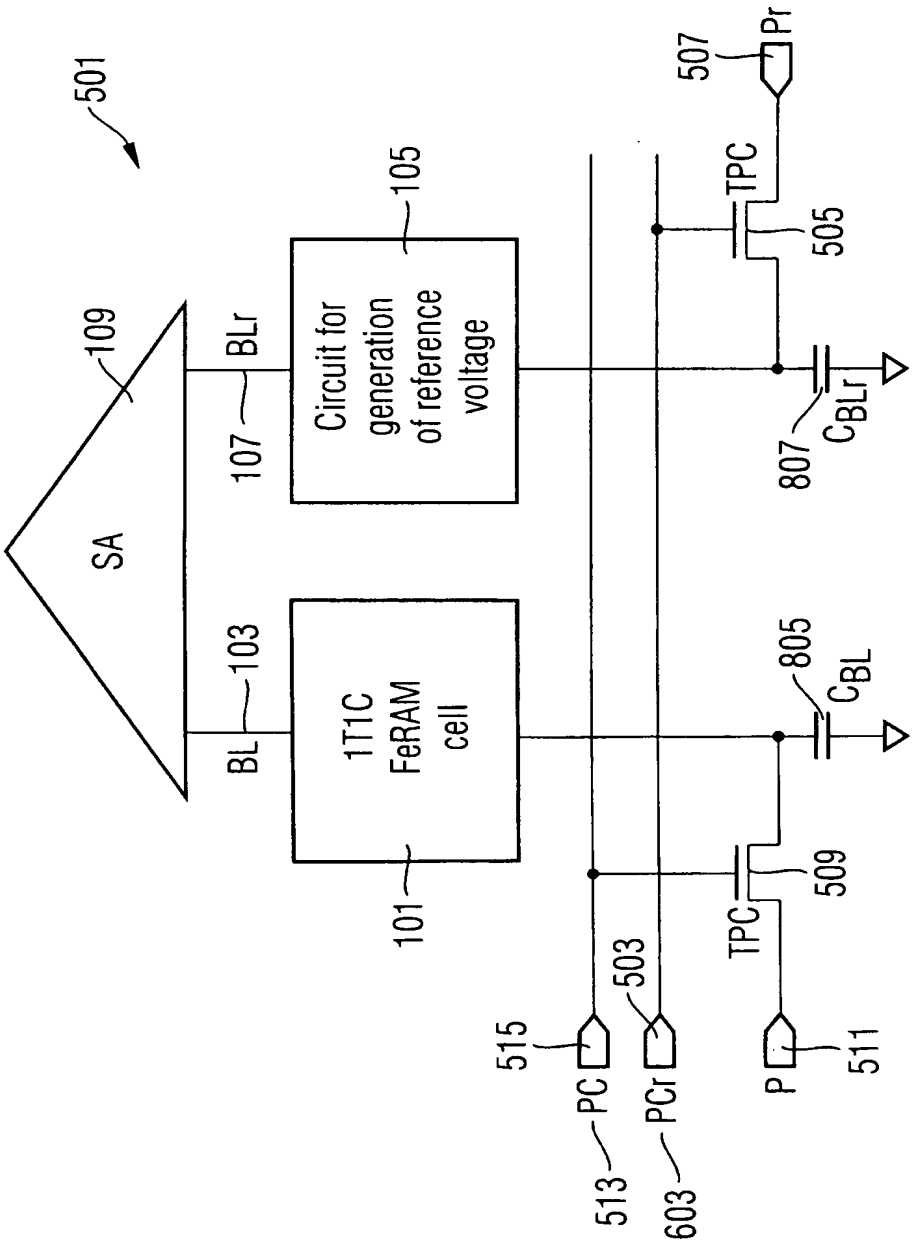
501
109
SA
BLr
107
BL
103
Circuit for generation of reference voltage
105
1T1C FeRAM cell
101
507
Pr
TPC
505
807
C_{BLr}
805
C_{BL}
TPC
509
515
PC
513
503
PCr
603
P
511

FIG 5

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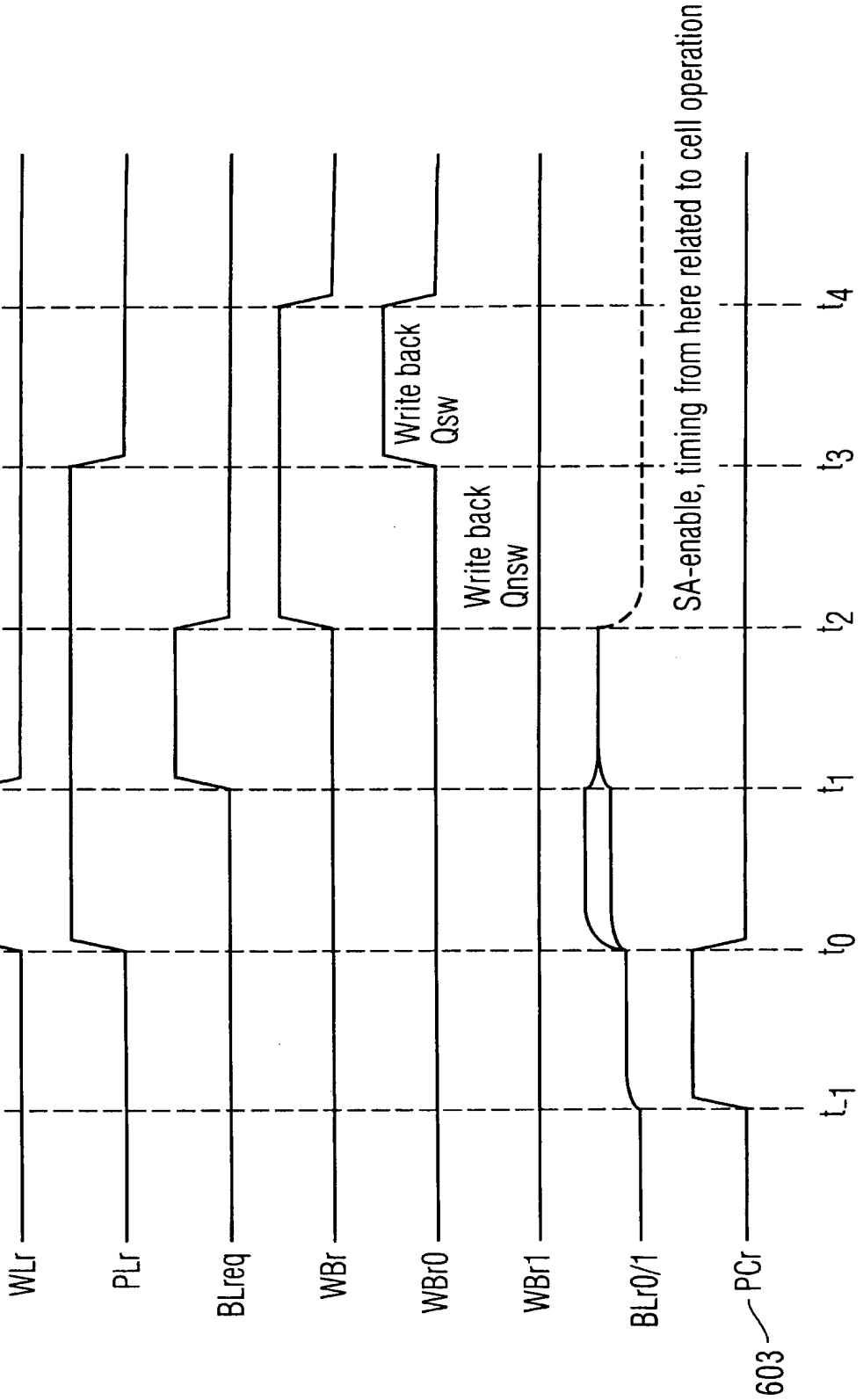
FIG 6


WLr
PLr
BLreq
WBr
WBr0
WBr1
BLr0/1
PCr
603
Write back Qsw
Write back Qnsw
SA-enable, timing from here related to cell operation
t-1
t0
t1
t2
t3
t4

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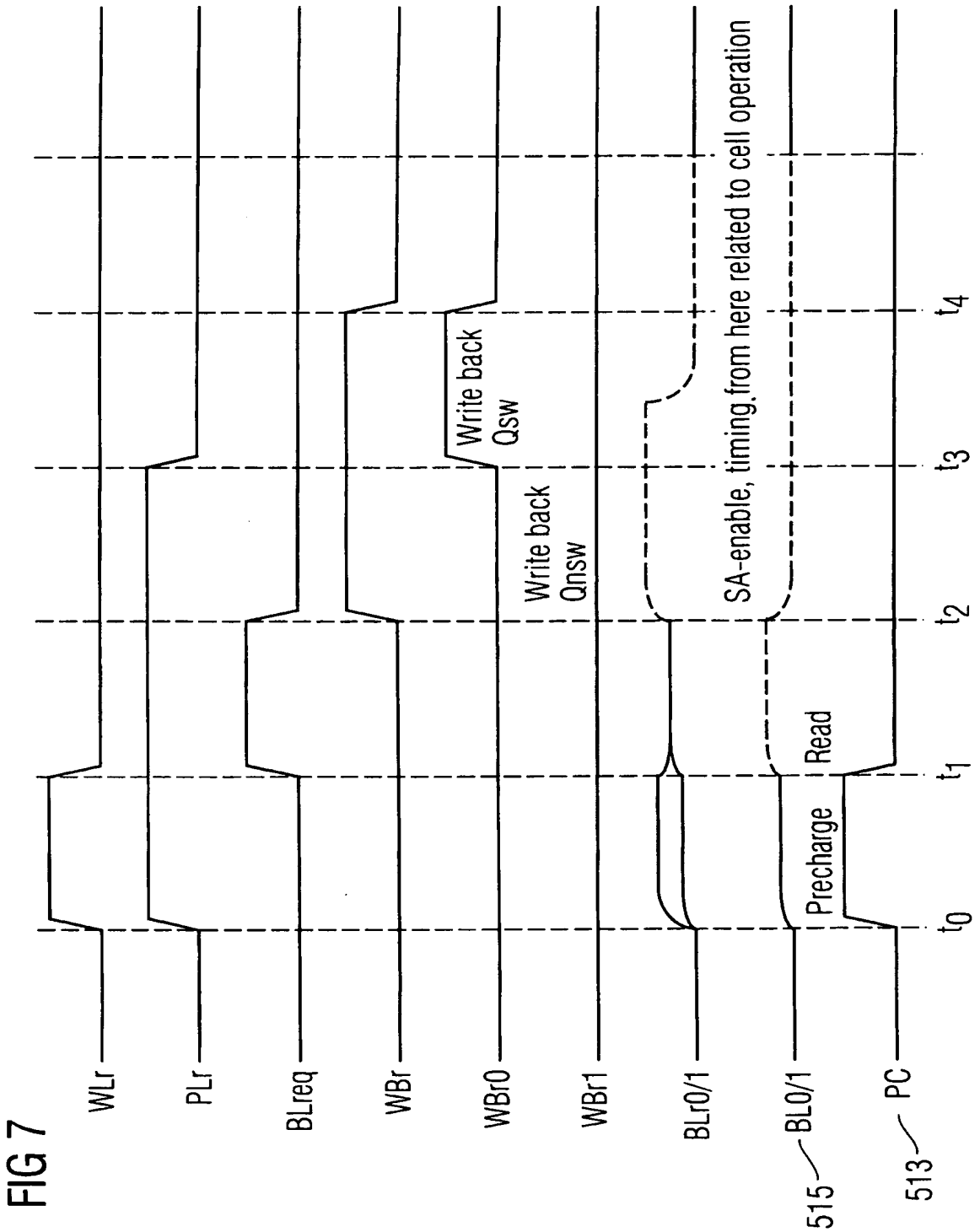
WLr
PLr
BLreq
WBr
WBr0
WBr1
BLr0/1
BL0/1
PC
515
513
Write back
Qsw
Write back
Qnsw
SA-enable, timing from here related to cell operation
Precharge
Read
t0
t1
t2
t3
t4

FIG 7

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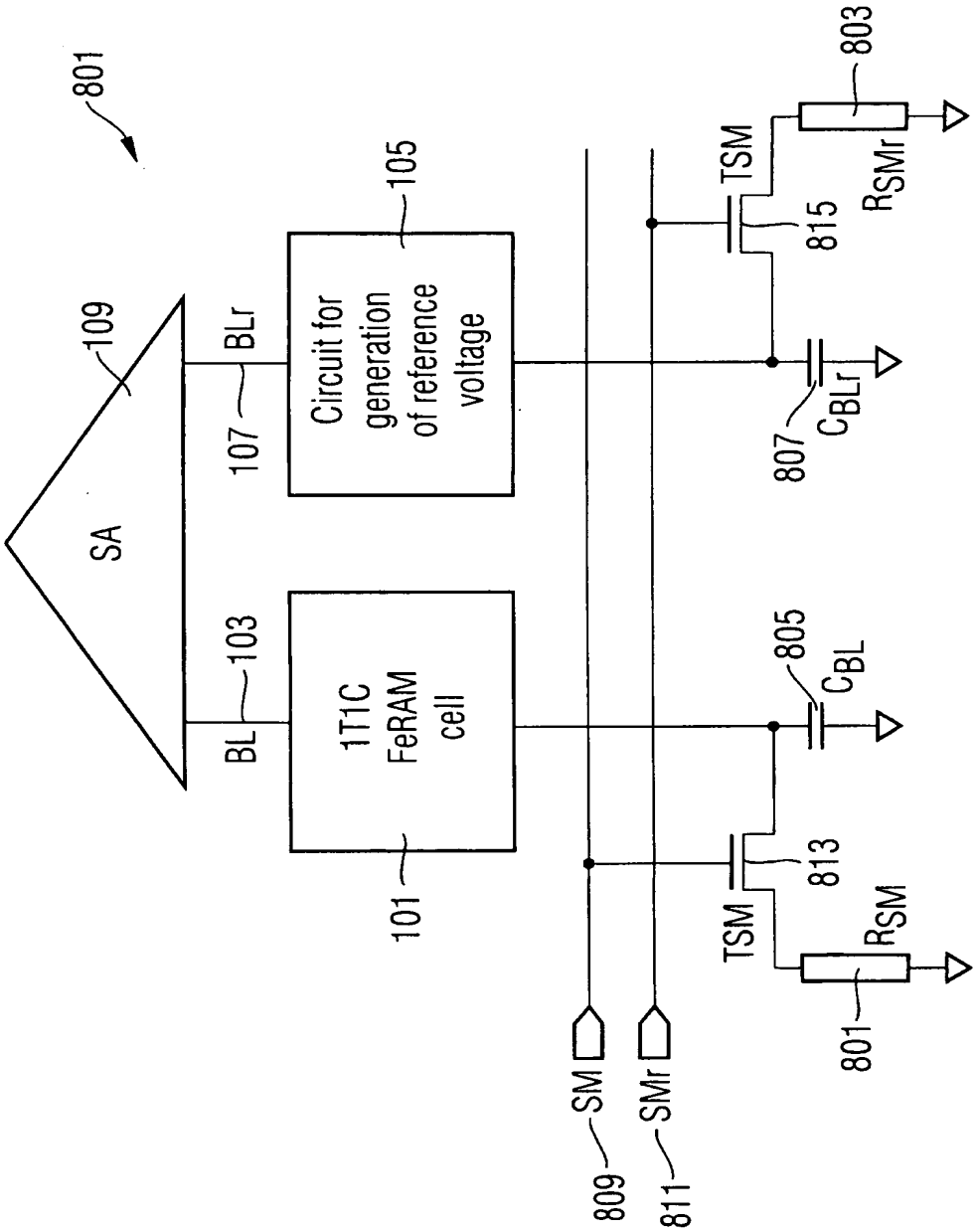
801
803
TSM
815
RSMr
105
109
BLr
107
Circuit for generation of reference voltage
SA
807
CBLr
103
BL
1T1C FeRAM cell
805
CBL
101
813
TSM
RSM
801
SM
SMr
809
811

FIG 8

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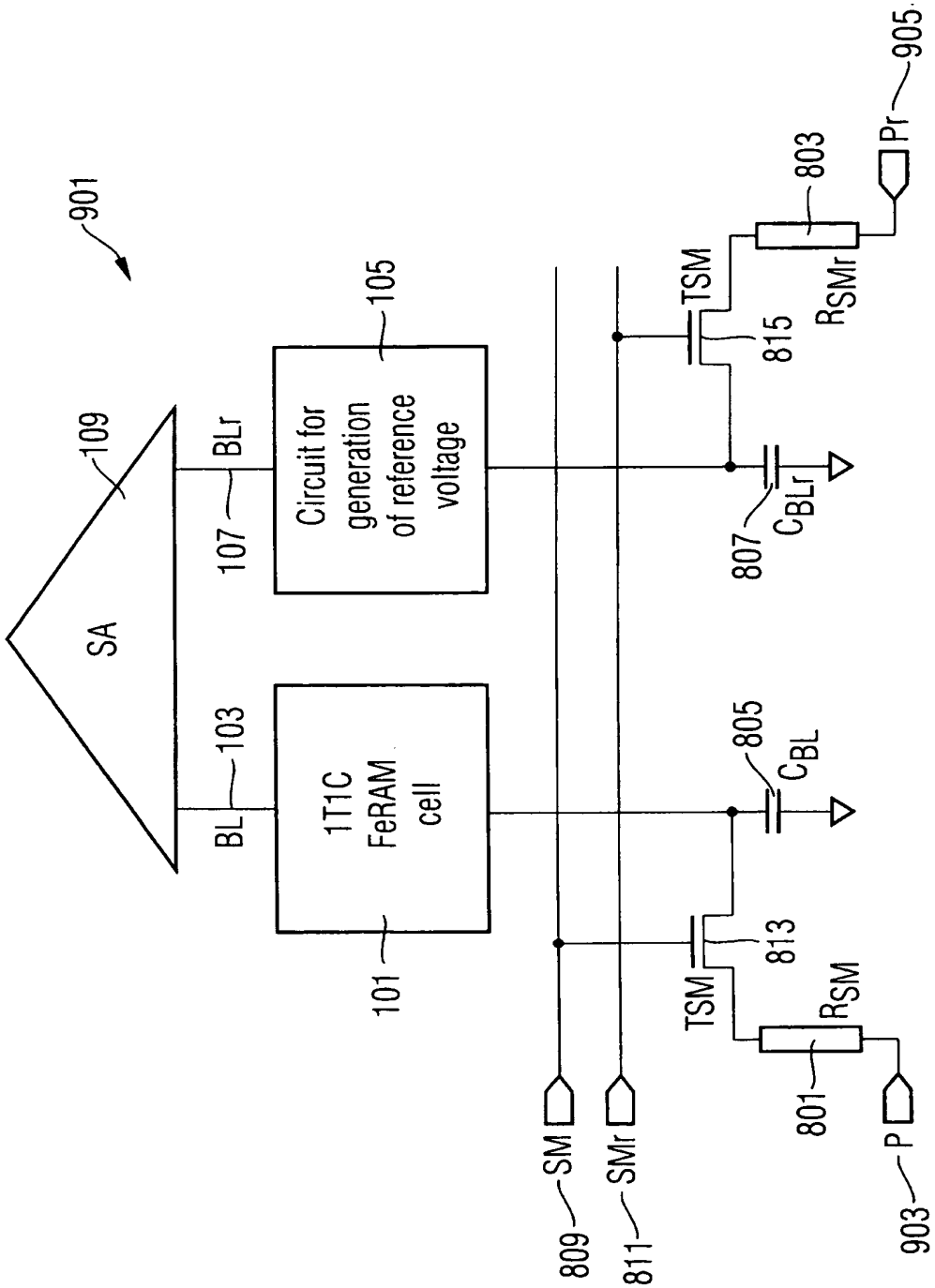
901
SA
109
BLr
107
Circuit for generation of reference voltage
105
BL
103
1T1C FeRAM cell
101
TSM
815
803
RSMr
Pr
905
807
CBLr
805
CBL
TSM
813
RSM
801
P
903
SM
809
SMr
811

FIG 9

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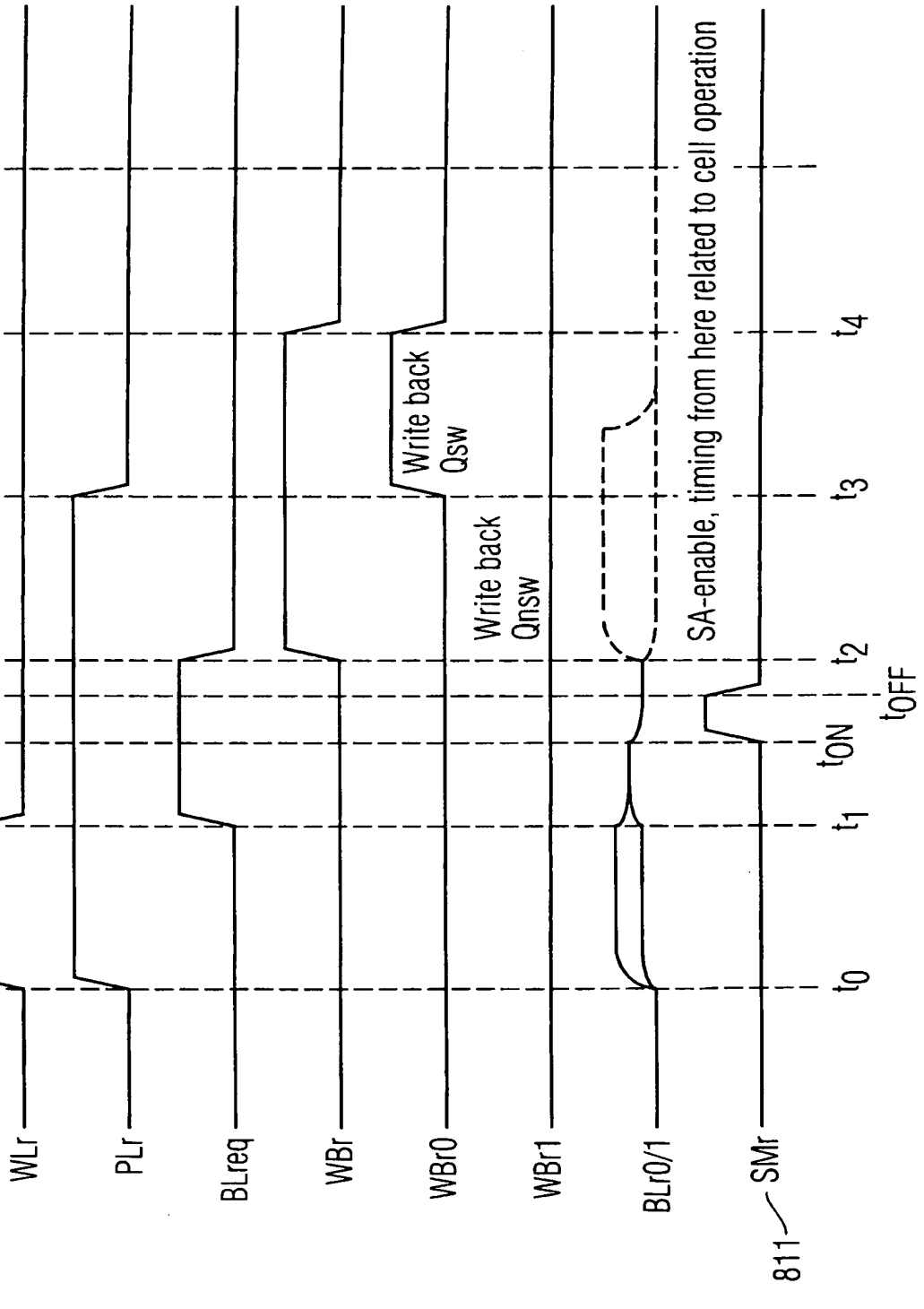
WLr
PLr
BLreq
WBr
WBr0
WBr1
BLr0/1
SMr
811
Write back Qsw
Write back Qnsw
SA-enable, timing from here related to cell operation
t0
t1
tON
t2
tOFF
t3
t4

FIG 10

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FIG 11

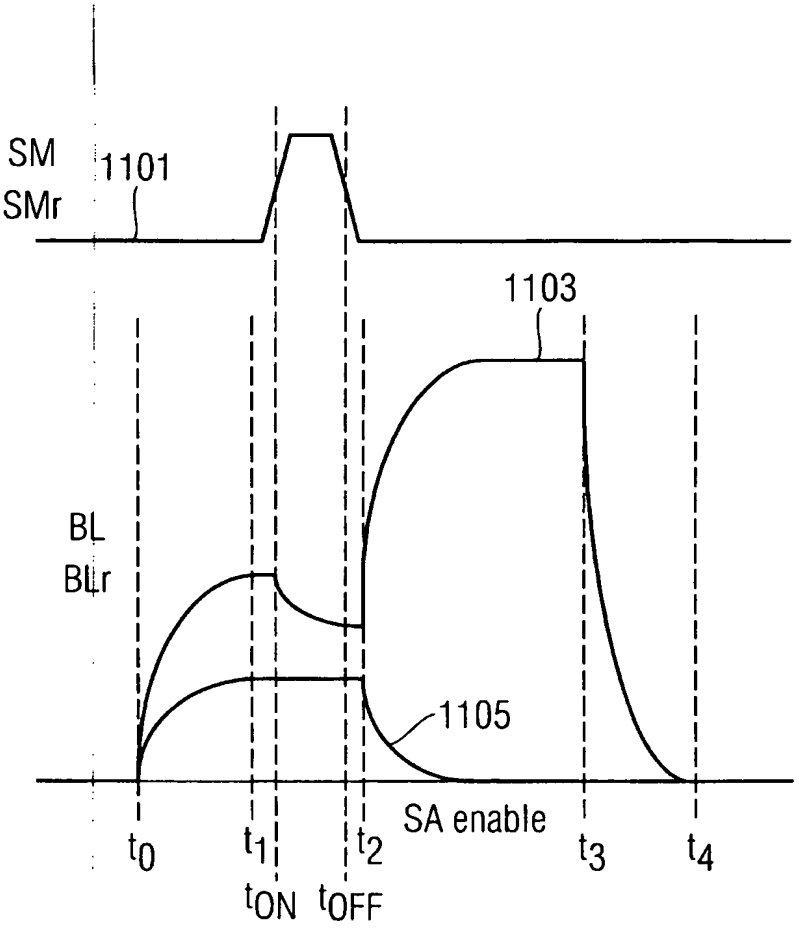

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FIG 12

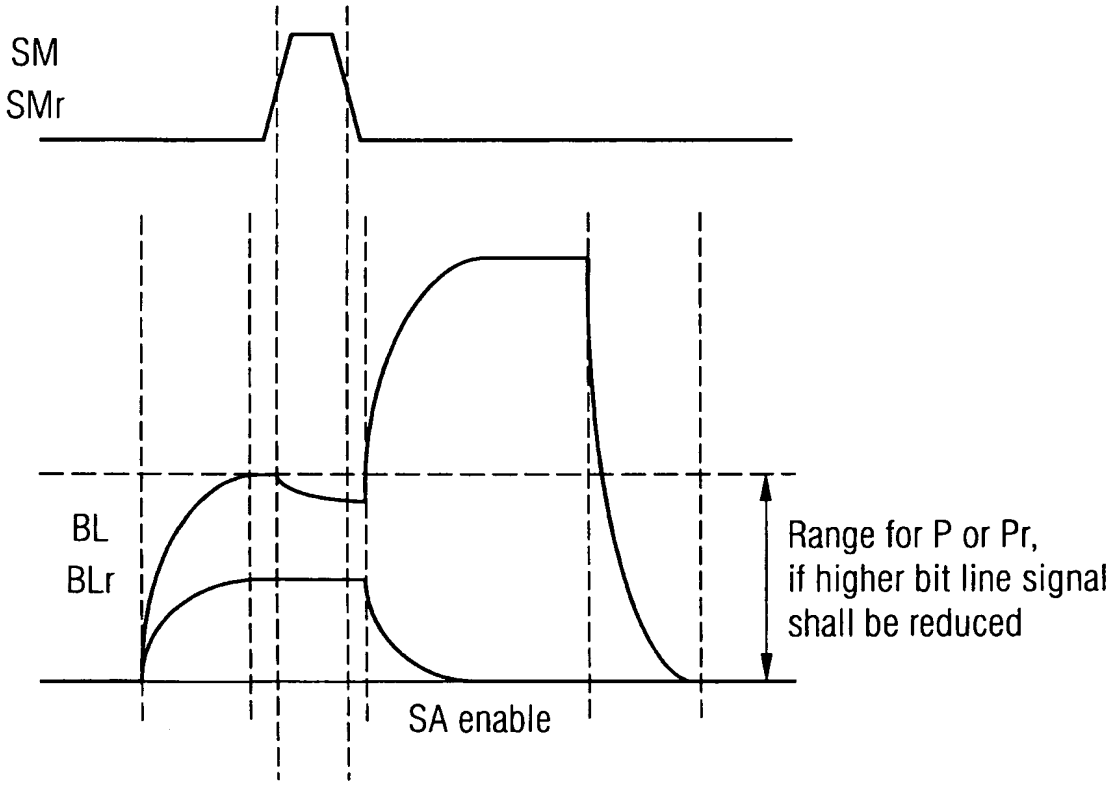
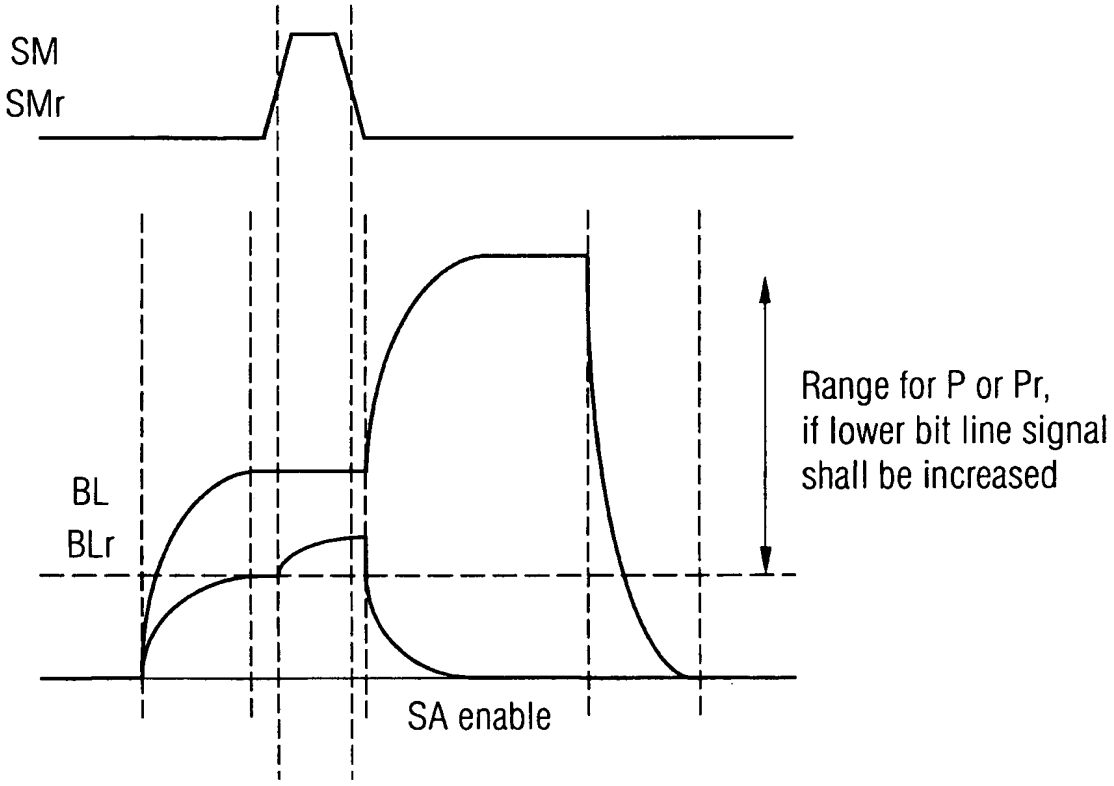

SM
SMr
BL
BLr
SA enable
Range for P or Pr,
if higher bit line signal
shall be reduced

FIG 13


SM
SMr
BL
BLr
SA enable
Range for P or Pr,
if lower bit line signal
shall be increased

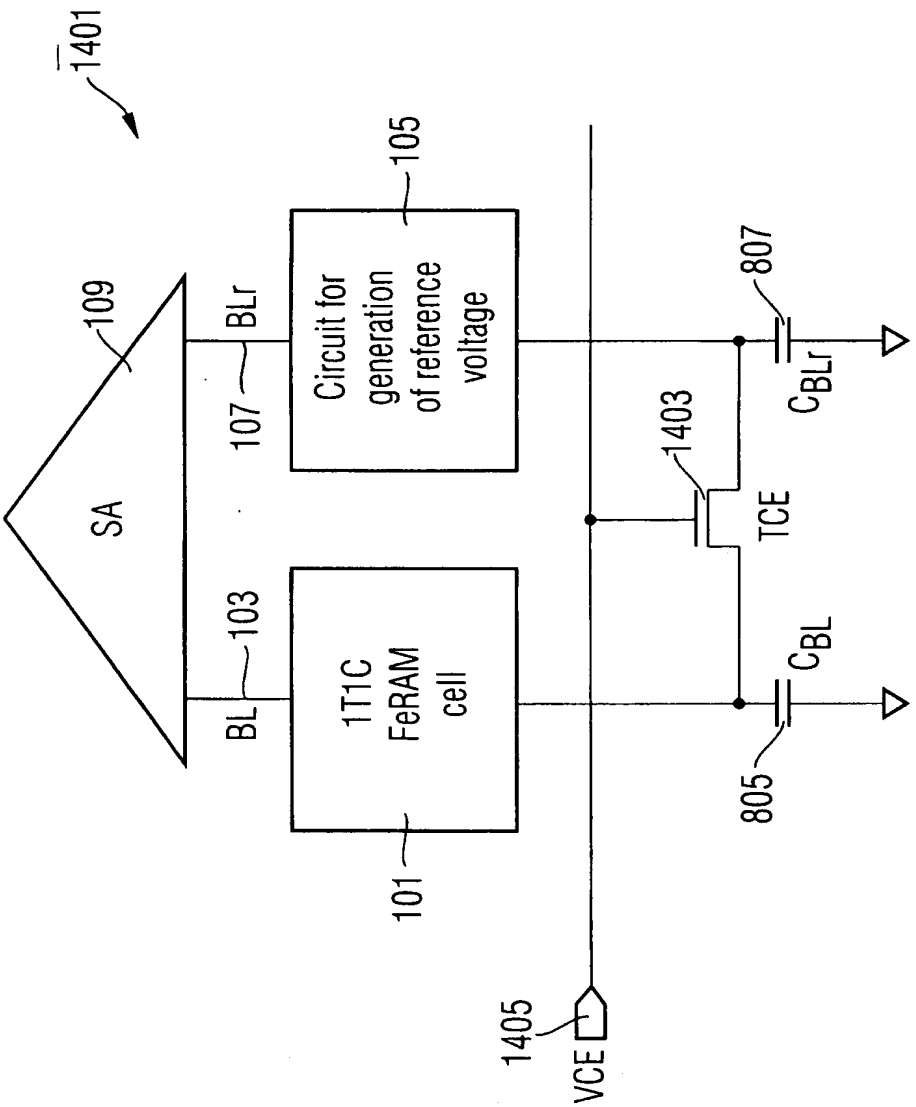

1401
105
109
BLr
Circuit for generation of reference voltage
807
107
SA
1403
TCE
C_{BLr}
103
BL
1T1C FeRAM cell
C_{BL}
805
101
1405
VCE

FIG 14

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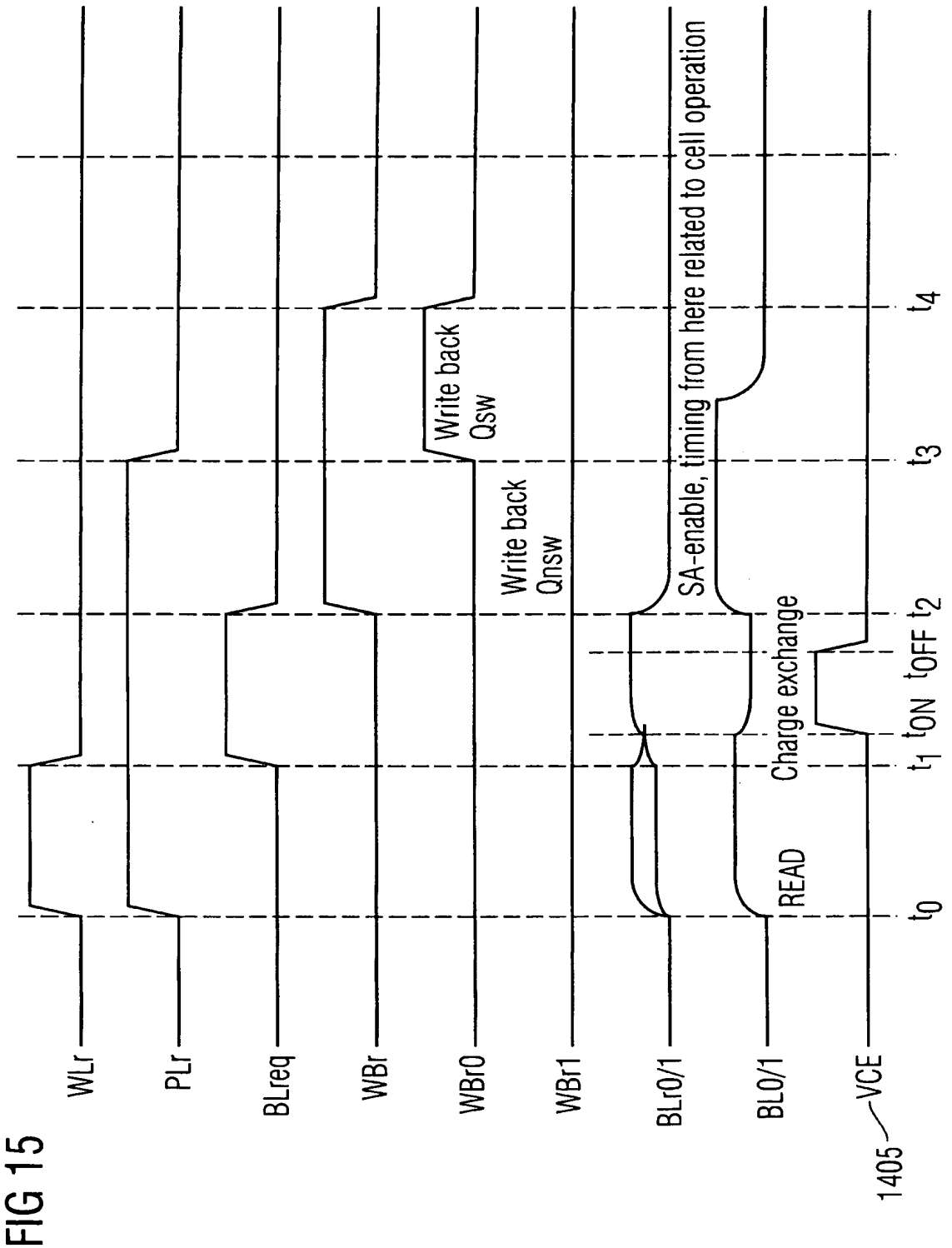
WLr
PLr
BLreq
WBr
WBr0
WBr1
BLr0/1
BL0/1
VCE
1405
Write back
Qsw
Write back
Qnsw
SA-enable, timing from here related to cell operation
Charge exchange
READ
t0
t1 tON tOFF t2
t3
t4

FIG 15

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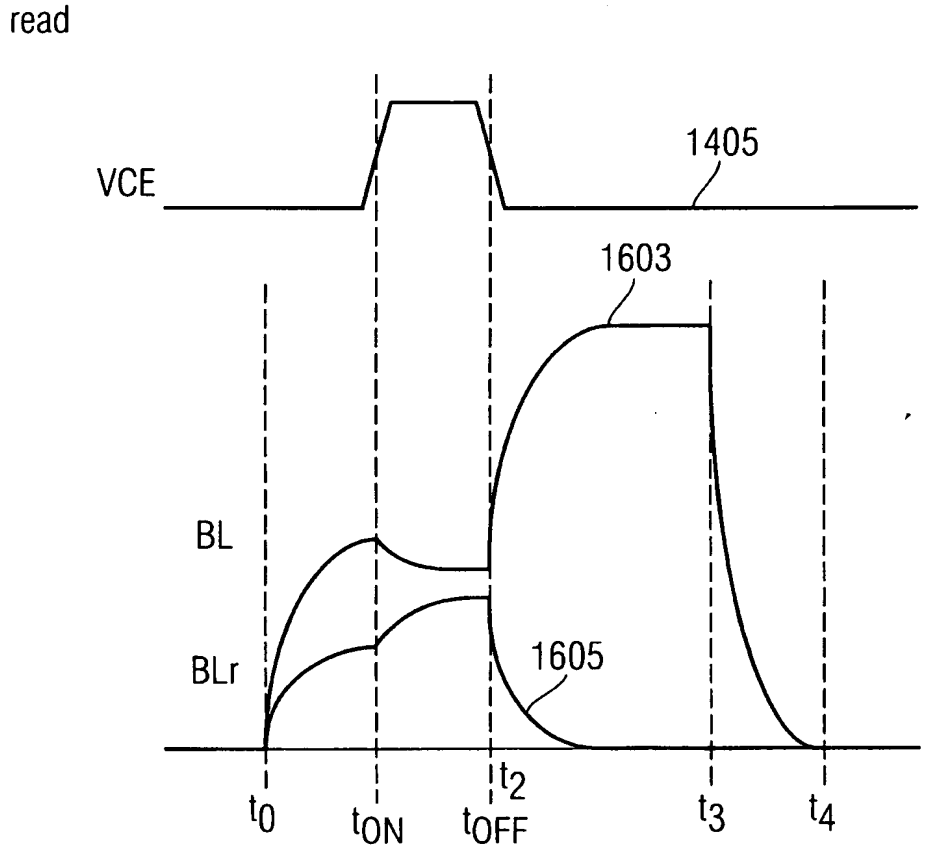
FIG 16



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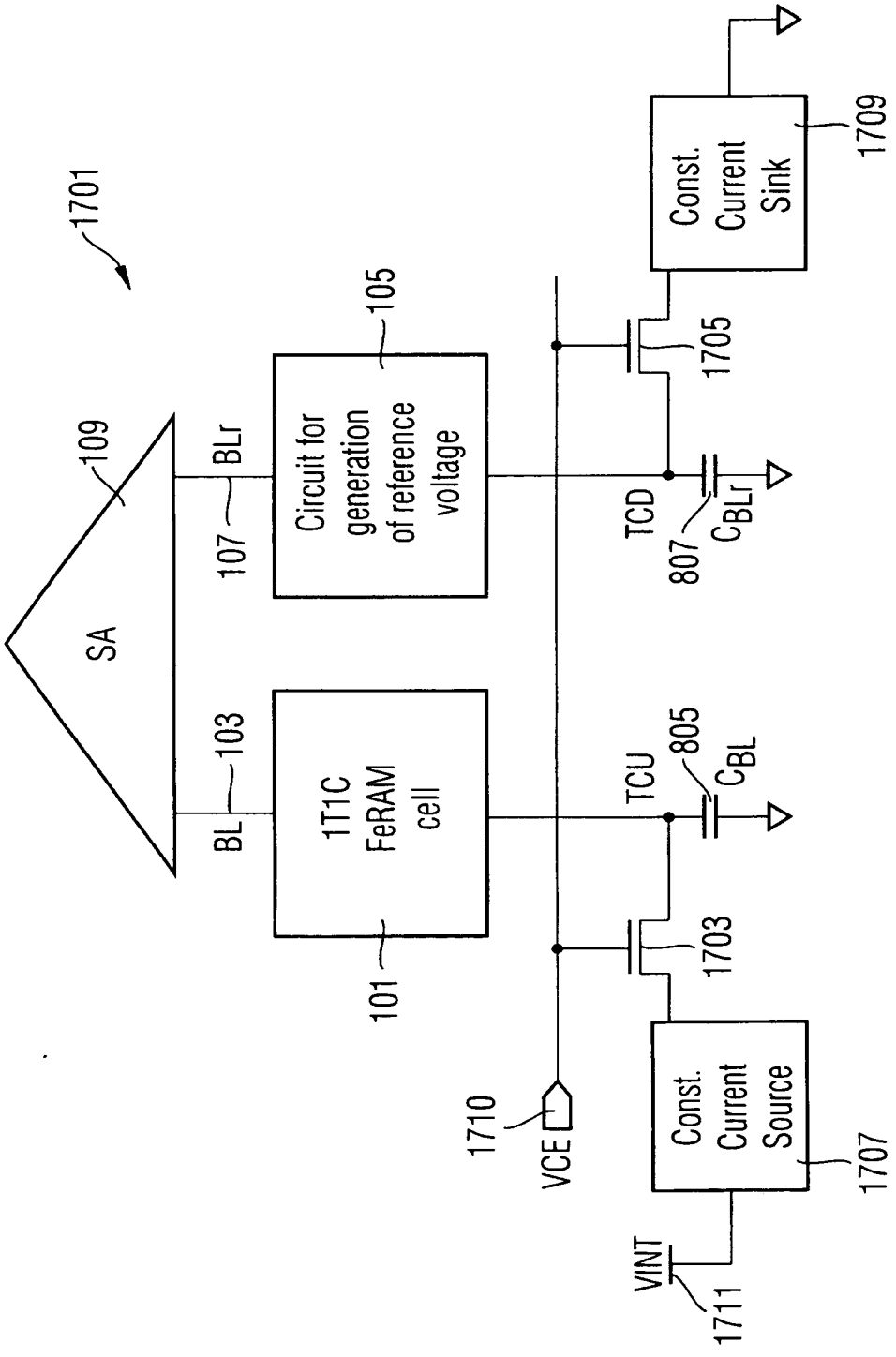
1701
109
SA
BLr
107
BL
103
Circuit for generation of reference voltage
105
1T1C FeRAM cell
101
Const. Current Sink
1709
1705
TCD
807
C_{BLr}
TCU
805
C_{BL}
1703
1710
VCE
Const. Current Source
1707
VINT
1711

FIG 17

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FIG 18

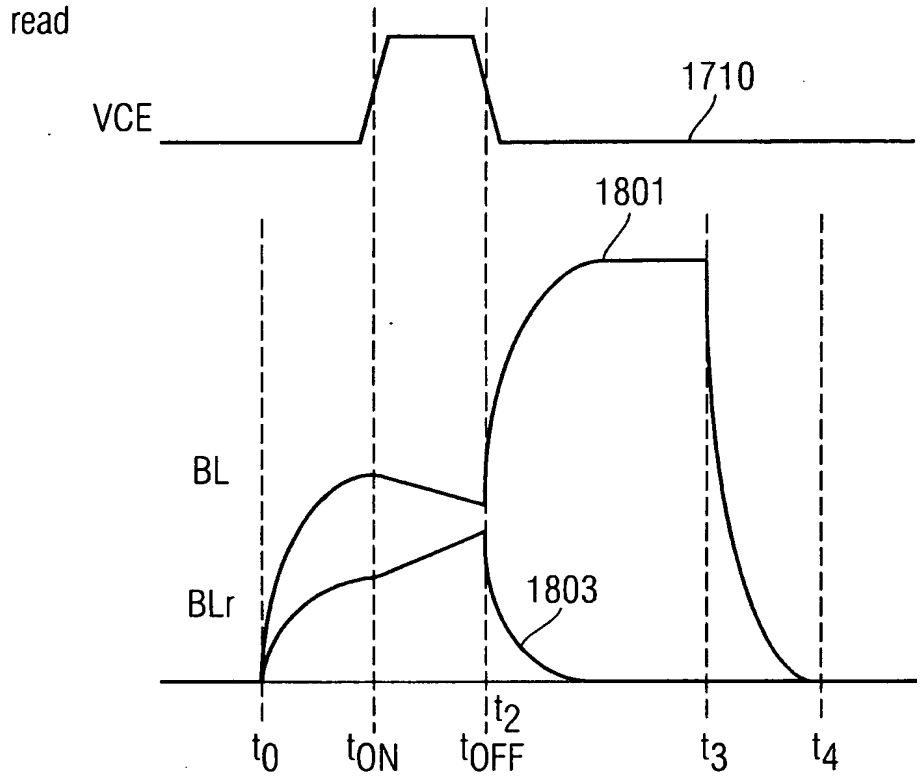

FIG 19